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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GUILL, RUSSELL L	
ART UNIT	**PAPER NUMBER**
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,816	CISCHKE, CHRISTOPHER M.	
	Examiner	Art Unit	
	Russ Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/20/2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 - 22 have been examined. Claims 1 - 22 have been rejected.

Specification

2. The Abstract is objected to for the following minor informality: The Abstract recites in lines 2 - 3, "that includes of creating". A piece appears to be missing.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. **Claims 9 - 16** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

a. The claims are directed to a digital storage medium having stored thereon a sequence of digital instructions to configure a computer. One interpretation of the claim is that the instructions are source code that configure the computer, and therefore the instructions are not executed, and therefore do not have functionality. The instructions may be interpreted as non-functional descriptive material, which is not statutory. A claim that can be interpreted so as to include both statutory and non-statutory interpretations must be amended to only include statutory material. Typically, when a computer-readable storage medium is claimed, the storage medium contains executable instructions that are executed on a computer or processor.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1 - 4, 6, 9 - 12, 14 and 17 - 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Oura (U.S. Patent Application Publication 2001/0001157) in view of Mobley (U.S. Patent Number 6,446,241).

a. The art of Oura is directed to a method of testing a cache (**Title and Abstract**).

b. The art of Mobley is directed to a method of testing a cache (**Title and Abstract**).

c. Regarding **claims 1, 9 and 17**:

d. Oura appears to teach:

i. Sequentially and randomly creating a series of functions (**figure 1, elements 10, 11 and 24; and figure 3, element S102; and figure 18, elements A and B**);

e. Oura does not specifically teach:

i. updating a data integrity buffer after each function of said series of functions is created;

ii. creating a series of integrity check functions from said data integrity buffer;

iii. writing said series of functions and said series of integrity check functions to a test file;

f. Mobley appears to teach:

i. updating a data integrity buffer after each function of said series of functions is created (**column 3, lines 1 - 6; it would have been obvious that the reference memory was a data integrity buffer**);

ii. creating a series of integrity check functions from said data integrity buffer (**column 3, lines 1 - 6; it would have been obvious to have integrity check functions since a reference memory is used to check the integrity of the transactions**);

iii. writing said series of functions and said series of integrity check functions to a test file (**column 13, lines 40 - 50; and column 14, lines 15 - 20; it would have been obvious to write the functions and integrity checks to a file since "low level test language source files" are generated by any kind of automatic test generator. Further, a cache tree file is formed to store a list of transactions**).

g. The motivation to use the art of Mobley with the art of Oura would have been the benefits recited in Mobley, including, that the invention provides a method to efficiently detect all legal cache states in a multilevel cache system (**column 2, lines 45 - 50**), and the invention has a cache system testbench that allows greater observability and can verify that every byte of data returned is correct (**column 6, 28 - 35**). the ordinary artisan would have recognized these elements as benefits that save time and cost.

h. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Mobley and the art of Wood with the art of Oura to produce the inventions of claims 1, 9 and 17.

i. Regarding **claims 2 and 10**:

j. Mobley appears to teach:

i. The data integrity buffer includes plurality of records, each record of said plurality of records including a cache memory address associated with contents of that cache memory address (**column 3, lines 1 - 6; it would have been obvious that the contents of the cache memory were stored associated with an address**).

k. Regarding **claims 3 and 11**:

l. Mobley appears to teach:

i. An address of each said record and contents of each said record are generated at random (**column 14, lines 1 - 2**).

m. Regarding **claims 4 and 12**:

n. Mobley appears to teach:

i. The data integrity buffer is updated after a normal function is created in said series of functions (**column 3, lines 2 - 3**).

o. Regarding **claims 6 and 14**:

p. Oura appears to teach:

i. Reading an entire test settings into an input buffer before the step of sequentially and randomly creating a series of functions, and further wherein the step of sequentially and randomly creating includes the step of using parameter data from the test settings to create said series of functions (**figure 1, element 13 and text to the right of element 13; and paragraph [0047]**).

q. Oura does not specifically teach:

i. Reading an entire test settings **file** into an input buffer before the step of sequentially and randomly creating a series of functions, and further wherein the step of sequentially and randomly creating includes the step of using parameter data from the test settings **file** to create said series of functions.

r. Mobley appears to teach:

i. A file (**column 13, lines 40 - 50**).

s. Regarding **claim 18**:

t. Oura appars to teach:

i. Means for providing test settings to said means for sequentially creating the series of instructions (**figure 1, element 13 and test to the right of element 13; and paragraph [0047]**).

u. Regarding **claim 19**:

v. Oura appears to teach:

i. the digital computer further includes a means for randomly generating an address of each record and contents of each record are generated at random (**figure 3, elements S102 and S103; and figure 4**).

w. Oura does not specifically teach (in **bold underline**):

i. **The data integrity buffer includes a plurality of records, each record including a cache memory address associated with contents of that cache memory address**, and further wherein the digital computer

further includes a means for randomly generating an address of each record and contents of each record are generated at random.

x. Mobley appears to teach:

i. The data integrity buffer includes a plurality of records, each record including a cache memory address associated with contents of that cache memory address (**column 3, lines 1 - 6**).

y. Regarding **claim 20**:

z. Oura does not specifically teach (in **bold underline**):

i. **Means for updating the data integrity buffer**.

aa. Mobley appears to teach:

i. Means for updating the data integrity buffer (**column 3, lines 1 - 6**).

bb. Regarding **claim 21**:

cc. Oura does not specifically teach (in **bold underline**):

i. **Means for updating the data integrity buffer includes means for updating the data integrity buffer after a normal function is created in said series of functions**.

dd. Mobley appears to teach:

i. Means for updating the data integrity buffer includes means for updating the data integrity buffer after a normal function is created in said series of functions (**column 3, lines 2 - 3**).

7. **Claims 5 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Oura as modified by Mobley as applied to claims **1 - 4, 6, 9 - 12, 14 and 17 - 21** above, further in view of Bourekas (U.S. Patent Number 5,386,579).

a. The art of Oura as modified by Mobley teaches a data integrity buffer having a plurality of records with an address and contents generated at random as recited in claims **1 - 4, 6, 9 - 12, 14 and 17 - 21** above.

b. The art of Bourekas is directed to a minimum pin count multiplexed addres and data bus system with a microprocessor and cache memory (**figure 1 and column 2, lines 5 - 35**).

c. The art of Bourekas and the art of Oura as modified by Mobley are analogous art because they both contain the art of accessing cache memory (**column 3, lines 28 - 35**).

d. Regarding **claims 5 and 13**:

e. Oura does not specifically teach:

i. At least one of the series of functions includes a bitwise memory write operation to a partial word cache memory location and wherein a corresponding integrity check function includes a bitwise memory read operation to read said partial word cache memory location.

f. Bourekas appears to teach:

i. At least one of the series of functions includes a bitwise memory write operation to a partial word cache memory location and wherein a corresponding integrity check function includes a bitwise memory read operation to read said partial word cache memory location (**column 4, lines 58 – 62, and column 5, lines 45 - 55**).

g. The motivation to use the art of Bourekas with the art of Oura as modified by Mobley would have been the benefits recited in Bourekas including that the invention allows low cost packaging while maintaining a variety of system capabilities (**column 2, lines 18 - 22**).

h. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Bourekas with the art of Oura as modified by Mobley to produce the claimed invention.

8. **Claims 7, 15 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Oura as modified by Mobley as applied to claims **1 - 4, 6, 9 - 12, 14 and 17 - 21** above, further in view of Azuma (U.S. Patent Application Publication 20040181655).

a. The art of Oura as modified by Mobley teaches a test settings file as recited in claims **1 - 4, 6, 9 - 12, 14 and 17 - 21** above.

b. The art of Azuma is directed to a processor having a cache memory and a process execution unit executing a process by use of information stored in the cache (Abstract).

c. The art of Azuma and the art of Oura as modified by Mobley are analogous art because they both contain the art of using cache memory.

d. Regarding **claims 7, 15 and 22**:

e. Oura does not specifically teach:

i. The test settings file includes data directing the generation of prefetch loops.

f. Azuma appears to teach:

i. data directing the generation of prefetch loops (**paragraph [0069]**).

g. The motivation to use the art of Azuma with the art of Oura as modified by Mobley would have been the benefits recited in Azuma including that it is advantageous to issue prefetch data by a prefetch instruction (**paragraph [0031]**).

h. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Azuma with the art of Oura as modified by Mobley to produce the claimed invention.

9. **Claims 8 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Oura as modified by Mobley as applied to claims **1 - 4, 6, 9 - 12, 14 and 17 - 21** above, further in view of Knuth (Donald E. Knuth, "The Art of Computer Programming", Volume 2/Seminumerical Algorithms, Third Edition, 1998, Addison Wesley Longman, pages 26 - 28).

a. The art of Oura as modified by Mobley teaches a data integrity buffer having a plurality of records with an address and contents generated at random as recited in claims **1 - 4, 6, 9 - 12, 14 and 17 - 21** above.

b. The art of Knuth is directed to generating random numbers (page 26).

c. The art of Knuth and the art of Oura as modified by Mobley are analogous art because they both contain the art of using random numbers (**Oura, figure 3, element S102**).

d. Regarding **claims 8 and 16**:

e. Oura does not specifically teach:

i. The address of each record and the contents of each record are generated at random using the Mitchell-Moore Additive generation method ().

f. Knuth appears to teach:

i. Numbers generated at random using the Mitchell-Moore Additive generation method (**page 27, last paragraph, and page 28**).

g. The motivation to use the art of Knuth with the art of Oura as modified by Mobley would have been the benefits recited in Knuth that the Mitchell-Moore generator is a much better type of additive generator than other linear congruential generators (**page 27, last paragraph**).

h. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Knuth with the art of Oura as modified by Mobley to produce the claimed invention.

10. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the Applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner. The entire reference is considered to provide disclosure relating to the claimed invention.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure:

a. David A. Wood et al.; "Verifying a multiprocessor cache controller using random test generation", August 1990, IEEE Design and Test of Computers, Volume 7, Issue 4, pages 13 - 25; teaches random test generation for testing a cache.

b. A. Chandra et al.; "AVPGEN - A Test Generator for Architecture Verification", June 1995, IEEE Transactions on Very Large Scale Integration Systems, Volume 3, Number 2, pages 188 - 200; teaches architecture verification by providing test inputs to a code design and comparing the output of the code design against a value calculated by the architecture.

c. Kawabe (U.S. Patent Number 6,968,520) teaches a design verification by using a random test, and comparing the output of the test with results obtained by functional simulation.

d. Hollander (U.S. Patent Application Publication 2005/0060132) teaches Verilog design verification by comparing simulated results against expected results.

e. Hollander (U.S. Patent Number 6,182,258) teaches Verilog design verification by providing input to a simulator and checking results against the output of a predictor simulator.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any

inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
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2/15/07
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